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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,251	09/25/2003	David F. Hepner	SJO920030029US1	5963
36380	7590	03/23/2006	EXAMINER	
RICHARD M. GOLDMAN 371 ELAN VILLAGE LANE SUITE 208, CA 95134			SUGENT, JAMES F	
			ART UNIT	PAPER NUMBER
			2116	
DATE MAILED: 03/23/2006				

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/671,251	<b>Applicant(s)</b> HEPNER ET AL.	
	<b>Examiner</b> James Sugent	<b>Art Unit</b> 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 September 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>16 March 2006</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

5 basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

10 (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15 Claims 1-4 and 11-14 are rejected under 35 U.S.C. 102(e) as being anticipated by .

Chakravarthy et al. (U.S. Patent Publication No. 2004/0059956 A1) (hereinafter referred to as Chakravarthy).

As to claim 1, Chakravarthy discloses a microprocessor system comprising a CPU (120), a clock (PLL 208) providing a CLK signal to the CPU (paragraph, lines 5-7), a counter (within  
20 performance monitor 204) counting clock pulses to the CPU (paragraph 28, lines 1-4), and a monitor (performance monitor 204), wherein the clock (208) is adapted to provide a CLK signal to the counter (via 210) when a software task is running on the CPU (paragraph 28), said counter adapted to count the number of clock pulses since a RESET (signal PMCPUCLKUNHALTED# 222) (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the  
25 performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted; paragraphs 27 and 28); the CPU is adapted (via PMON circuit 200.2) to provide a RESET signal (PMCPUCLKUNHALTED# 222) to the counter for

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each CLK pulse when a software task is not running on the CPU (Chakravarthy discloses the counter within the performance monitor 204 does not count the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is de-asserted; paragraph 28); and the monitor is adapted to store the value in the counter immediately prior to the last RESET (Chakravarthy saving the counted clock pulses as “Time0” when a CPU\_CLKS\_UNHALTED event occurs; paragraph 36).

As to claim 2, Chakravarthy discloses the microprocessor system wherein the CPU is adapted (via PMON circuit 200.2) to block a RESET signal (PMCPUCLKUNHALTED#) to the counter when a software task is running on the CPU (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted; paragraphs 27 and 28).

As to claim 3, the microprocessor system wherein the CPU is adapted to continuously pass CLK signals (via 210) to the counter when a software task is running on the CPU (paragraphs 27 and 28).

As to claim 4, Chakravarthy discloses the microprocessor system wherein the CPU is adapted to pass a RESET signal (via PMON circuit 200.2) to the counter when is software task is not running on the CPU (paragraphs 26-28).

As to claim 11, Chakravarthy discloses a method of operating a microprocessor system, said system comprising a CPU (120), a counter (within performance monitor 204; paragraph 28, lines 1-4), a monitor (performance monitor 204), and a clock (PLL 208), and wherein the clock (208) provides a CLK signal train to the counter (via 210) while a software task is running on the CPU (paragraph 28), the counter counting the number of clock pulses since a RESET (signal

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PMCPUCLKUNHALTED# 222) (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted ;paragraphs 27 and 28), the CPU providing (via PMON circuit 200.2) a RESET signal (PMCPUCLKUNHALTED# 222) to the counter for each CLK pulse when a software task is not running on the CPU (Chakravarthy discloses the counter within the performance monitor 204 does not count the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is de-asserted; paragraph 28), and the monitor storing the value of the counter prior to the last RESET (Chakravarthy saving the counted clock pulses as “Time0” when a CPU\_CLKS\_UNHALTED event occurs; paragraph 36).

As to claim 12, Chakravarthy discloses the method wherein the CPU blocks (via PMON circuit 200.2) the RESET signal (PMCPUCLKUNHALTED#) to the counter when a software task is running on the CPU (Chakravarthy discloses when a clock signal is asserted to CPU 120, the counter within the performance monitor 204 counts the number of clock pulses (or ticks) when said PMCPUCLKUNHALTED# is asserted; paragraphs 27 and 28).

As to claim 13, Chakravarthy discloses the method wherein the CPU continuously passes CLK signals (via 210) to the counter when a software task is running on the CPU (paragraphs 27 and 28).

As to claim 14, Chakravarthy discloses the method wherein the CPU passes a RESET signal (via PMON circuit 200.2) to the counter when is software task is not running on the CPU (paragraphs 26-28).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

5 (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10 Claims 5-10 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravarthy et al. (U.S. Patent Publication No. 2004/0059956 A1) (hereinafter referred to as Chakravarthy) as applied to claims 1 and 11 above, and further in view of Terrell, II (U.S. Patent Publication No. 2004/0098631 A1) (hereinafter referred to as Terrell).

As to claim 5, Chakravarthy does not disclose the monitor of the microprocessor system  
15 is adapted to output a control signal responsive to monitor content.

Terrell teaches a system clock power management system wherein a clock controller (10 or 62) is adapted to output control signals (14) to processors within the system (20 and 24 or 50 and 52) to control the common clock to the processors dependent on processor usage and clock counts when processor is active (paragraphs 15 and 32).

20 It would have been obvious to one of ordinary skill of the art having the teachings of Chakravarthy and Terrell, at the time the invention was made to modify the performance monitor of Chakravarthy to include the ability to send control signals in response to monitored activity as taught by Terrell. One of ordinary skill in the art would be motivated to make this combination in order to give the ability of the performance monitor to output control signals in view of the  
25 teachings of Terrell, as doing so would give the added benefit of monitoring both common and shared processor clock usage between multiple processors instead of one (paragraphs 9 and 10).

As to claim 6, Terrell teaches the microprocessor system wherein the monitor is adapted to output a power control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

5 As to claim 7, the microprocessor system wherein the monitor is adapted to output a function control signal responsive to monitor content (Terrell teaches a method and system wherein the output control signals from the monitor circuit [clock controller] are in response to hardware interrupts received from the system; paragraph 46).

10 As to claim 8, the microprocessor system wherein the monitor is adapted to output a clock control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 9, the microprocessor system wherein the monitor is adapted to output a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold ("guard band" frequency) (paragraphs 13 and 53).

15 As to claim 10, the microprocessor system wherein the monitor is adapted to output a control signal reducing clock pulse input to the CPU responsive to count content when the monitor content is below a threshold (paragraph 53).

As to claim 15, Chakravarthy does not disclose the monitor of the method wherein the monitor outputs a control signal responsive to count content.

20 Terrell teaches a system clock power management system wherein a clock controller (10 or 62) is adapted to output control signals (14) to processors within the system (20 and 24 or 50 and 52) to control the common clock to the processors dependent on processor usage and clock counts when processor is active (paragraphs 15 and 32).

It would have been obvious to one of ordinary skill of the art having the teachings of Chakravarthy and Terrell, at the time the invention was made to modify the performance monitor of Chakravarthy to include the ability to send control signals in response to monitored activity as taught by Terrell. One of ordinary skill in the art would be motivated to make this combination in order to give the ability of the performance monitor to output control signals in view of the teachings of Terrell, as doing so would give the added benefit of monitoring both common and shared processor clock usage between multiple processors instead of one (paragraphs 9 and 10).

As to claim 16, the method wherein the monitor outputs a power control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 17, the method wherein the monitor outputs a function control signal responsive to monitor content (Terrell teaches a method and system wherein the output control signals from the monitor circuit [clock controller] are in response to hardware interrupts received from the system; paragraph 46).

As to claim 18, the method wherein the monitor outputs a clock control signal responsive to monitor content (Terrell discloses controlling the clock frequency to the processing elements thus controlling power; paragraph 15).

As to claim 19, the method wherein the monitor outputs a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold (“guard band” frequency) (paragraphs 13 and 53).



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As to claim 20, the method wherein the monitor outputs a control signal reducing clock speed of the CPU responsive to monitor content when the monitor content is below a threshold (paragraph 53).

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

20 James Sugent  
Patent Examiner, Art Unit 2116  
March 16, 2006

  
**LYNNE H. BROWNE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2100**